

PAJDC

<b>QUERY CONTROL FORM</b>		<b>RTIS USE ONLY</b>	
Application No.	<u>09/827,073</u>	Prepared by	<u>NH</u>
Examiner-GAU	<u>Phan - 2818</u>	Date	<u>3-29-4</u>
		No. of queries	<u>1</u>
			<u>IFW</u>

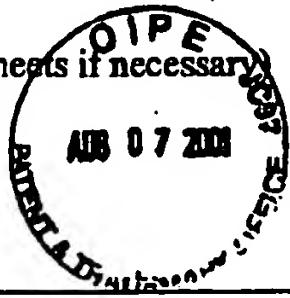
<b>JACKET</b>					
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449		
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b		
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract		
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs		
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other		

<b>SPECIFICATION</b>	<b>MESSAGE</b>	
	PTO-1449: Please either initial or line through citations. Copy provided for reference	
<b>CLAIMS</b>	<b>RESPONSE</b>	
	initials NH	
	Thank you	
<b>RESPONSE</b>	DONE	

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE  
(REV. 7-80) PATENT AND TRADEMARK OFFICE

**LIST OF PRIOR ART  
CITED BY APPLICANT**

(Use several sheets if necessary)



Atty. Docket No.

Y0R920000587US1 (13958)

Serial No.

09/827,073

**RECEIVED**

AUG 09 2001

Technology Center 2100

Group 2818

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL*	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
AA						
AB						
AC						
AD						
AE						
AF						
AG						
AH						
AI						
AJ						

**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
						YES

**OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

TP	"An 8ns Random Cycle Embedded RAM Macro with Dual-Port Interleaved DRAM Architecture (D <sup>2</sup> RAM)", Yasuhiro Agata et al, 2000 IEEE International Solid-State Circuits Conference, 9 pages.

EXAMINER	Trong Phan	DATE CONSIDERED	4/9/04
----------	------------	-----------------	--------

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and do not consider. Include copy of this form with next communication to applicant.